WHAT IS CLAIMED IS:

1. A demodulation apparatus for a communication system, comprising:

an analog-to-digital converter device to convert an intermediate frequency signal into a digital signal and provide a quadrature component and an in-phase component of the digital signal;

a plurality of filters to filter components of the digital signal outputted from the analog-to-digital converter device in a low pass band respectively; and

a CDMA modem to demodulate outputs of the plurality of filters.

2. The apparatus of claim 1, wherein said analog-to-digital converter comprises:

a digital sampler to sample the intermediate frequency signal;

a zero-order hold device to determine an amplitude of the sampled intermediate frequency signal;

a quantizer to convert the sampled intermediate frequency signal processed by the zero-order hold device to a digital signal;

a plurality of latches to transmit the digital signal from the quantizer to a plurality of channels after a prescribed time delay; and

a plurality of output formatters to periodically output the latched digital signal transmitted to corresponding channels of the plurality of channels.

3. The apparatus of claim 2, wherein each of said plurality of output formatters comprises:

a plurality of negators to negate the latched digital signal and output a negated latched signal; and

a plurality of selectors one to one coupled to each of the plurality of negators to select and output one of the negated latched signal and an unprocessed latched digital signal.

4. The apparatus of claim 3, wherein the plurality of output formatters comprise first and second output formatters, and wherein the output of each output formatter is received by a low pass filter.

5. The apparatus of claim 1, wherein the plurality of channels comprise an In-phase channel and a Quadrature channel.

6. An analog-to-digital converter, comprising:

a digital sampler to sample an intermediate frequency signal;

a zero-order holder to determine an amplitude of the sampled intermediate frequency signal;

a quantizer to convert the sampled intermediate frequency signal processed by the zero-order holder to a digital signal;

a plurality of latches to transmit the digital signal to a plurality of channels after a prescribed time delay; and

a plurality of output formatters to periodically output the latched digital signal transmitted to corresponding channels of the plurality of channels.

7. The apparatus of claim 6, wherein each of said plurality of output formatters comprises:

a plurality of negators to negate the latched digital signal and output a negated latched signal; and

a plurality of selectors to select and output one of the negated latched signal and an unprocessed latched digital signal.

8. The apparatus of claim 7, wherein the plurality of output formatters comprise a first and second output formatter, and wherein the output of each output formatter is received by a low pass filter.

9. The apparatus of claim 6, wherein the plurality of channels comprise an I channel and a Q channel.

10. A signal processor, comprising:

a digitizer, which receives and analog signal and generates a digital signal;

a channel separator, which receives the digital signal from the digitizer and separates the digital signal into at least 2 channels, each channel having a different phase; and

a phase shift controller, which receives a clock signal and controls the phase shifting of the channel separator.

11. The signal processor of claim 10, wherein the channels comprise a Q channel and an I channel having a phase difference of approximately 90°.

12. The signal processor of claim 10, wherein the analog signal is an intermediate frequency CDMA formatted signal.

13. The signal processor of claim 12, wherein an output of the signal processor is a QPSK modulated digital signal, having a first component and a second component out of phase with the first component.

14. The signal processor of claim 10, wherein the channel separator comprises:

a latch circuit, which receives the digital signal and outputs a first signal and a second signal, wherein the second signal is a delayed first signal;

an output formatter, which receives the first and second signals and outputs the first and second signals at prescribed periods.

15. The signal processor of claim 14, wherein the latch circuit comprises a first latch, a second latch, and a third latch, wherein the output formatter comprises a first output formatter and a second output formatter, and wherein the first latch receives the digital signal from the digitizer, the second latch receives the output of the first latch and provides the first signal to the first output formatter and the third latch, and the third latch provides the second signal to the second output formatter.

16. The signal processor of claim 15, wherein the phase shift controller provides the clock signal to the first, second, and third latches to control the phase shifting, and provides a control signal to the first and second output formatters to control output periods.

17. The signal processor of claim 15, wherein the first and second output formatters each comprise:

a plurality of negators, which receive and negate the corresponding first or second signal; and

a plurality of selectors to select and output one of the negated signal from the negator and the corresponding first or second signal, wherein each one of the plurality of negators is coupled to one of the plurality of selectors.

18. The signal processor of claim 10, wherein the digitizer comprises

a sampler, which receives and samples the analog signal;

a zero order hold circuit, which receives an output of the sampler and determines an amplitude of the received signal; and

a quantizer, which receives an output of the zero order hold circuit and generates the digital signal.

19. The signal processor of claim 10, wherein the phase shift controller comprises:

a plurality of buffers to receive and forward the clock signal; and

a logic circuit responsive to a buffered clock signal to generate a control signal to control an output of the channel separator.

20. The signal processor of claim 10, further comprising a plurality of Finite Impulse Response (FIR) filters coupled to receive an output of the channel separator, wherein an individual FIR filter is coupled to each channel of the at least two channels.

21. A demodulator for a CDMA receiver, comprising:

an input circuit to amplify a filtered CDMA formatted input signal;

a first signal processor to generate an intermediate frequency CDMA signal based on the amplified input signal;

a second signal processor to output first and second digital signals on first and second channels, respectively, based on the intermediated frequency CDMA signal, said second signal processor having an analog-to-digital converter to convert the intermediate frequency CDMA signal to an intermediate digital signal and a channel separator to generate the first and second digital signals based on the intermediate digital signal; and

an output circuit to output a demodulated output signal based on the first and second digital signals, said output circuit having first and second Finite Impulse Response (FIR) filters to receive and filter the first and second digital signals, respectively, wherein the first and second digital signals have different phases.

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